CLAIMS:

1. A FIFO-register comprising a sequence of register cells, which register cells comprise a data section and a status section, in which data provided at an input is shifted via the data sections in the register cells to an output, the status section of each cell indicating whether the data section of that cell contains valid data, wherein the status section of the cells comprises

- a clock input for receiving an input clock signal,
- a status input for receiving an input status signal,
- a status output for providing an output status signal,
- a clock output for providing an output clock signal,
- a first charge controlling element coupled to the status input,
- a second charge controlling element coupled to the status output,
- a control unit coupled to the status input, to the status output and to the clock input, for generating the output clock signal, which output clock signal controls the charge controlling elements and the data section, wherein the status output of a status section shares a node with the status input of its successor for dynamic storage.

2. A FIFO-register according to claim 1, wherein the control unit comprises a first combination unit for combining the input status signal and the output status signal, and for providing in response to these signals an intermediate signal to a second combination unit, which combines the intermediate signal with the input clock signal and generates the output clock signal.

3. A FIFO-register according to claim 1, wherein the data section of the cell comprises a data input, a data output, a clock input for receiving the output clock signal from the clock output of the status section, the data output being coupled via a first chain to a first voltage line and via a second chain to a second voltage line, the first chain comprising the main current path of a first semiconductor element which is controlled by the data input, and a second semiconductor element which is controlled by the clock input, and the second chain

comprising the main current path of a third semiconductor element which is controlled by the data input, and a fourth semiconductor element which is controlled by the clock input.

4. A FIFO-register according to claim 1, wherein the data section of the cell shares a capacitive node with the data section of a successor for storage of the data.

5. A digital signal processor comprising a first functional unit, and a second functional unit and a FIFO-register according to one of the previous claims for transferring data between the first and the second functional unit.